a data output terminal;

read means for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to said data output terminal; and

compression means for carrying out a prescribed logical operation on said data read by said read means from said plurality of memory cells in response to a test mode designating signal for compressing said data to one-bit data and externally outputting the same.

2. (Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of data output terminals;

a plurality of read means provided [respectively for] corresponding to said plurality of data output terminals for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to corresponding data output terminals in response to said clock signal;

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a plurality of compression means [respectively] provided [to said plurality of] corresponding to each respective read means for carrying out a prescribed logical operation on said data read by corresponding read means from said plurality of memory cells thereby compressing said data to one-bit data; and

output means for generating outputs of respective compression means to corresponding data output terminals.

3. (Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of data output terminals;

a plurality of read means provided [respectively] corresponding to said plurality of data output terminals for simultaneously reading data from a predetermined plurality of memory cells in response to a read mode command incorporated in synchronization with said clock signal;

compression means for carrying out a prescribed logical operation on said data read by said plurality of read means from said memory cells for compressing said data to one-bit data; and

output means for generating an output of said compression means to a particular one of said plurality of data output terminals.

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4. (Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks each having a memory cell [arrays and having] array;

activation means provided for the banks for activating and precharging [corresponding said] the memory [cells] arrays on a bank by bank basis;

a data output terminal provided in common for said plurality of banks;

read means provided for each of said plurality of banks for simultaneously reading data from a predetermined plurality of memory cells from a corresponding memory cell array in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to said data output terminal in response to said clock signal;

a plurality of first compression means provided [respectively for] corresponding to the banks and each said first compression means for carrying out a prescribed logical operation on said data read by corresponding read means from said plurality of memory cells in an activated bank for compressing said data to one-bit data; and

second compression means for carrying out another prescribed logical operation on outputs of said plurality of first compression

means for compressing said outputs to one-bit data and externally outputting the same to said data output terminal.

Cont. A1

5. (Amended) A synchronous semiconductor memory device incorporating external signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks each having a memory cell [arrays and having] array;

activation means provided corresponding to the banks and for activating and precharging corresponding memory [cells] arrays, on a bank by bank basis;

a plurality of data output terminals shared by said plurality of banks;

a plurality of read means provided [respectively] corresponding to said plurality of data output terminals [of] in each said bank for simultaneously reading data from a predetermined plurality of memory cells from a corresponding memory cell array in response to a read mode command incorporated in synchronization with said clock signal for successively transferring said data to corresponding data output terminals in response to said clock signal;

a plurality of first compression means provided [respectively for said] corresponding to the respective banks for carrying out a first logical operation on said data read by each of said plurality

of read means from said memory cells in each said bank for compressing said data to one-bit data; and

second compression means for carrying out a second logical operation on outputs of said plurality of first compression means for compressing said outputs to one-bit data and externally outputting the same.

6. (Amended) A synchronous semiconductor memory device incorporating external signals including address signals and control signals in synchronization with a clock signal formed of a series of pulses, said synchronous semiconductor memory device comprising:

a plurality of banks each including a memory cell [arrays, and having] array ~~with each memory cell array~~ having a plurality of memory cells, each bank including means for [activating and precharging corresponding said memory cells on bank by bank basis; and] selecting a memory cell designated by an address signal incorporated in synchronization with said clock signal;

first activation means responsive to a bank address signal designating a bank incorporated in synchronization with said clock signal for activating a bank designated by said bank address signal, independently of the states of activation and precharging of remaining banks in a normal mode of operation, and

second activation means for simultaneously activating said plurality of banks in response to a test mode designating signal.

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10. (Amended) A [synchronous] semiconductor memory device comprising:

a memory cell array having a plurality of memory cells;

read means for simultaneously reading data of a prescribed number of memory cells from said memory cell array;

a first wired circuit having a plurality of n-channel insulated gate type field effect transistors each having a gate receiving [said] each respective data read by said read means from said prescribed number of memory cells, said plurality of n-channel insulated gate type field effect transistors being connected [to] between a first signal line and a first potential node in parallel with each other;

a second wired circuit provided separately from said first wired circuit and having a plurality of p-channel insulated gate type field effect transistors each having a gate receiving [said] each respective data read by said read means from said prescribed number of memory cells, said p-channel insulated gate type field effect transistors connected [to] between a second signal line and a second potential node in parallel with each other; and

logic means coupled to receive signals on said first and second signal lines for carrying out a prescribed logic operation on outputs of said first and second wired circuits.

Claim 11, line 15 (last line of page 87), after "said" insert --first--.

9 ~~12~~. (Amended) A synchronous type semiconductor memory device operating in synchronization with a clock signal, comprising:

data output means for externally supplying [applied] received data in synchronization with said clock signal;

a memory cell array having a plurality of memory cells;

selection means responsive to an address signal [applied] received in synchronization with said clock signal for simultaneously selecting a predetermined number of said memory cells in said memory cell array,

said predetermined number being a multiple of [the] a number of data bits [by] which said data output means can externally [supplied] supply at a time;

read means responsive to a read mode designating signal [applied] received in synchronization with said clock signal for simultaneously reading and storing data of said predetermined number of memory cells selected by said selection means; and

compression means responsive to a test mode designating signal designating a test mode of operation for compressing the data of the predetermined number of cells stored in said read means to a one-bit data indicating whether or not a defective memory cell is included in said predetermined number of memory cells for external outputting.

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~~16~~. (Amended) The device according to claim ~~12~~, wherein said compression means includes;

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gate means responsive to a precharge enable signal being inactive for generating test data corresponding to the data stored in said read means,

first wired circuit including a plurality of first conductivity type field effect transistors provided respectively for said test data and having gates receiving corresponding test data and provided between a first signal line and a first fixed potential [mode] node in parallel with each other, and a second conductivity type field effect transistor responsive to said precharge enable signal for precharging said first signal line to a second fixed potential,

a second wired circuit including a plurality of second conductivity type field effect transistor provided respectively for said test data and having gates receiving corresponding test data and provided between a second signal line and [the] a second fixed potential node in parallel with each other, and a precharge transistor of the first conductivity type for precharging said second signal line to the fixed potential of said first fixed potential node in response to said precharge enable signal, and

generation means responsive to said precharge enable signal being inactive for determining whether signal potentials on said first and second signal lines are identical in logic to each other to generate said one-bit data indicating the result of determination.

Claim 21, line 2, after "includes" insert --a--.

Claim 24, line 2, change "units" to --unit--.

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~~32~~. (Amended) The device according to claim ~~30~~, wherein [the set of means] elements associated with said memory cell array and [the set of additional means] elements associated with said another memory array respectively form banks each accessed on a bank by bank basis, and wherein said synchronous type semiconductor memory device further comprises means responsive to said test mode designating signal for activating all said banks.

REMARKS

In response to the Office Action dated January 11, 1995, claims 1-5, 9-12, 16, 21, 24 and 32 are amended. Claims 1-5 and 9-33 are now active in this application. Care has been exercised to avoid the introduction of new matter.

A drawing correction is proposed for Figs. 10-12, 15, 16, 18, 19, 23, 38 and 39 to apply a bracket to gather all traces to a common figure. A separate paper requesting approval is submitted concurrently herewith.

REJECTION OF CLAIMS UNDER 35 U.S.C. § 112, SECOND PARAGRAPH

Claims 2, 4, 9 and 11-33 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. In support of this position, the Examiner identifies several phrases that are deemed

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